REMARKS

The Examiner's Action mailed on November 26, 2008, has been received and its contents carefully considered.

In this Amendment, Applicants have amended claims 1 and 3. Claims 1 and 3 are the independent claims, and claims 1 and 3 remain pending and under consideration in the application, claims 5-8 having been withdrawn and claims 2 and 4 having been cancelled without prejudice. For at least the following reasons, it is submitted that this application is in condition for allowance.

Claims 1-4 were rejected under 35 U.S.C. §102(b) as being anticipated by *Yamada* (US 4,654,685). This rejection is respectfully traversed.

Claims 1 and 3 have been amended to add the following features (a), (b) and (c):

(a) The "second surface side region and the second substrate side region are completely separated from each other by means of the second dividing region".

(For support, see page 25, lines 19-22 of the specification as filed: "Therefore, the second surface side region **7A** and the second substrate side region **7B** are completely separated from each other by means of the second dividing region **10** ...".)

(b) The "third surface side region and the third substrate side region are completely separated from each other by means of the third dividing region".

(For support, see page 26, lines 21-24 of the specification as filed: "Therefore, the third surface side region **8A** and the third substrate side region **8B** are completely separated from each other by means of the third dividing region **11** ...").

(c) The "first to third photoelectric conversion regions are arranged in a direction parallel to the semiconductor substrate".

(See FIGS. 2 and 5 of the application as filed).

Yamada does not teach or suggest features (a), (b) and (c) as recited above.

Regarding features (a) and (b), each of the n conductivity bands **15R**, **15G**, **15B**, **16R**, **16G** and **16B** of *Yamada* are discontinuous, and an upper portion and a lower portion of each of the p-type layers **14R**, **14G** and **14B** are not completely separated from each other by means of the n conductivity band (see FIGS. 2, 6, 13 and 14 of *Yamada*).

Thus, *Yamada* neither teaches or suggests either feature (a), wherein "the second surface side region and the second substrate side region are completely separated from each other by means of the second dividing region", nor feature (b), wherein "the third surface side region and the third substrate side region are completely separated from each other by means of the third dividing region".

As for feature (c), the Office Action does not appear to have given patentable weight to the feature of "the element dividing region dividing the

photoelectric conversion layer into a first photoelectric conversion region, a second photoelectric conversion region, and a third photoelectric conversion region along the semiconductor substrate" in claims 1 and 3 as originally filed. In order to clarify this feature, as well as continuing to recite "the element dividing region dividing the photoelectric conversion layer into a first photoelectric conversion region, a second photoelectric conversion region, and a third photoelectric conversion region", claims 1 and 3 have been amended to then recite feature (c), i.e. wherein "the first to third photoelectric conversion regions are arranged in a direction parallel to the semiconductor substrate".

In the photoelectrical conversion panel of *Yamada*, the top layer **B**, the middle layer **G** and the bottom layer **R** are arranged perpendicularly to the p-type conductivity layer **11R**. Owing to this arrangement, the bottom layer **R**, the middle layer **G** and the top layer **B** have to be formed one by one in a manufacturing process of the photoelectrical conversion panel (see FIGS. 2, 6, 13 and 14 of *Yamada*).

On the other hand, feature (c) provides the advantage that the first to third photoelectric conversion regions (aside from the first to third dividing regions) in the present invention can be formed simultaneously. See FIGS. 6A to 6C and the corresponding description from page 36, line 24 to page 38, line 8 of the specification as filed:

First, n-type impurities (e.g., arsenic (As)) are applied onto one surface of the silicon substrate **2**, and an $n^{\square}$ type common electrode layer **3** is formed on the surface part of the silicon substrate **2** (see FIG. 6A). The common electrode layer **3** may be formed by applying arsenic glass onto one surface of the silicon substrate **2** and by diffusing arsenic from this arsenic glass into the silicon substrate **2**.

Thereafter, a $p^{\square}$ type photoelectric conversion layer **4** having a thickness of 6μm to 8μm is formed on the common electrode layer **3** according to epitaxial growth (see FIG. 6B).

Thereafter, n-type impurities (e.g., phosphorus (P)) are injected into a predetermined area of the photoelectric conversion layer **4** from the surface thereof through an opening of a resist film having predetermined patterns. The n-type impurities are then diffused into the depths of the photoelectric conversion layer **4**, and an n-type diffusion dividing region **5B** is formed. The n-type impurities are allowed to reach an interface between the common electrode layer **3** and the photoelectric conversion layer **4** by the diffusion. As a result, the diffusion dividing region **5B** connected to the common electrode layer **3** is obtained. The diffusion dividing region **5B** is exposed on the surface of the photoelectric conversion layer **4**.

Further, according to a known LOCOS technique, a predetermined area of the surface part of the diffusion dividing region **5B** is selectively oxidized, thus forming an oxide film **5A**. The width of the oxide film **5A** is made to be smaller than the width of, for example, the diffusion dividing region **5B**, in this case, after forming the oxide film **5A**, the diffusion dividing region **5B** is exposed around the oxide film **5A**. The photoelectric conversion layer **4** is divided into the first, second, and third photoelectric conversion regions **6**, **7**, and **8** by means of the element dividing region **5** including the oxide film **5A** and the diffusion dividing region **5B**. This state is shown in FIG. 6C.

More particularly, as the top layer **B**, the middle layer **G** and the bottom layer **R** in *Yamada* are arranged perpendicularly to the p-type conductivity layer **11R**, they are therefore not "arranged in a direction parallel to the semiconductor substrate" as recited in claims 1 and 3.

Thus, *Yamada* also fails to teach or suggest "the element dividing region dividing the photoelectric conversion layer into a first photoelectric conversion region, a second photoelectric conversion region, and a third photoelectric conversion region, wherein the first to third photoelectric conversion regions are

arranged in a direction parallel to the semiconductor substrate" as also recited in claims 1 and 3.

Consequently, claims 1 and 3 patentably define over *Yamada* and are allowable, claims 2 and 4 having been cancelled.

It is submitted that this application is in condition for allowance. Such action and the passing of this case to issue are requested.

Should the Examiner feel that a conference would help to expedite the prosecution of this application, the Examiner is hereby invited to contact the undersigned counsel to arrange for such an interview.

No remittance is believed to be due. Should any fee be required, however, the Commissioner is hereby authorized to charge the fee to our Deposit Account No. 18-0002, and advise us accordingly.

Respectfully submitted,

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Date

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